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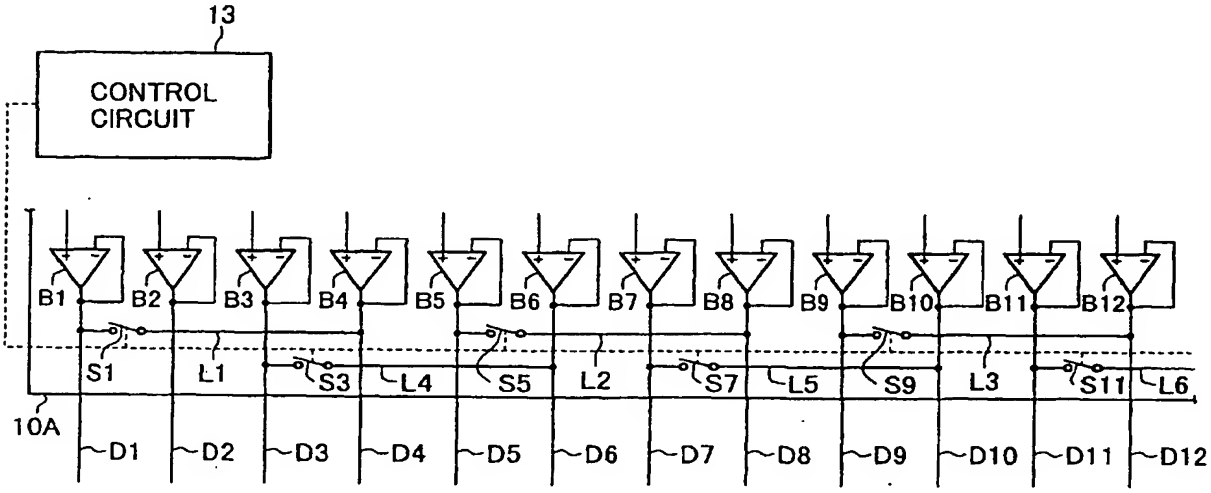
(54) Dot-inversion data driver for liquid-crystal display device

(57) In an LCD driven by a data driver 10A of a dot-inversion driving type, the outputs of voltage buffer amplifiers B1 to B12 are connected to respective data-bus lines D1 to D12 of the LC panel. The data-bus lines carry different colour signals; short-circuiting switches S1, S3, S5, S7, S9 and S11 are connected between successive pairs of data-bus lines concerned with the same display colour, and interconnecting lines L1, L2, L4 for the switches are arranged in a staggered configuration on first and second rows. These short-circuiting switches can be formed in a space-saving manner on one side of every other data-bus line, and turned on by a control circuit 13 when the outputs of the voltage buffer amplifier are in a high impedance state, i.e. in a blanking period.

FIG.4



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EP 1 202 245 A2

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Description

[0001] The present invention relates to a data driver for a liquid-crystal display device, having voltage buffer amplifiers, which output analog gradation voltages. The analog gradation voltages are applied to data-bus lines such that voltage polarities of adjacent data-bus lines concerned with the same display colour are opposite to each other. More particularly, the invention relates to a data driver for driving the data-bus lines of a liquid-crystal display device in a dot-inversion fashion with respect to time and space.

[0002] **FIG. 8** shows the output stage of a prior-art data driver 10X connected to the data-bus lines of a liquid-crystal display (LCD) panel.

[0003] The voltage buffer amplifiers B1 to B12 of the data driver 10X are respective voltage followers, and the outputs thereof are connected to the respective data-bus lines D1 to D12 of the LCD panel. The data driver 10X drives the data-bus lines in a dot-inversion fashion with respect to time and space. That is, voltages applied to adjacent data-bus lines at the same time have opposite polarities to each other, and analog gradation voltages corresponding to the display data are output from the respective voltage buffer amplifiers B1 to B12 such that voltage polarity of each data-bus line is opposite to that of the adjacent lines. According to the dot-inversion driving technique, variations in the potential of a pixel electrode caused by cross capacitance between a data-bus line and a scan-bus line can be effectively cancelled and, further, the common potential applied to the opposite electrode can be stabilized, resulting in a reduced flicker.

[0004] However, charge and discharge currents of each of the voltage buffer amplifiers B1 to B12 are relatively large, leading to a higher power consumption.

[0005] Facing such a disadvantage, in order to utilize the electric charge accumulated on the data-bus lines effectively, and thus decrease power consumption, short-circuiting switches S1 to S12 are connected between a common line CL and the respective data-bus lines D1 to D12. When the outputs of the voltage buffer amplifiers B1 to B12 have been brought into a high impedance state during a horizontal blanking period, the short-circuiting switches S1 to S12 are simultaneously turned on. The potentials of the data-bus lines D1 to D12 are thereby rendered nearly equal to the common potential of the opposite plane electrode of the liquid-crystal display panel, enabling the current consumed in the voltage buffer amplifiers B1 to B12 to decrease by up to a half.

[0006] However, since it is necessary to provide the short-circuiting switches next to the respective voltage buffer amplifiers, the area of the data driver 10X increases, thereby lowering the density of data-bus lines in the arrangement.

[0007] **Fig. 9** shows a data driver 10Y of a dot-inversion driving type disclosed in JP 10-282940 A.

[0008] In this circuit, adjacent data-bus lines are connected in pairs by short-circuiting switches S1 to S9. With this circuit, since the number of the short-circuiting switches is reduced to half that of Fig. 8, the above described problem can be solved.

[0009] However, since different colour signals are carried by adjacent bus lines, there is no correlation therebetween and the efficiency of utilization of electric charge accumulated on the data-bus lines. For example, the potentials of the data-bus lines D1 to D6 are distributed in a horizontal period as shown in **Fig. 10,** and when the short-circuiting switches S1, S3 and S5 turn on in the next horizontal blanking period, the potentials are distributed as shown in **Fig. 11** producing differences between the potential of each data-bus line and the common potential VCOM of the opposite electrode. This increases the power consumption of the data driver 10Y compared with the data driver 10X of Fig. 8. Further, the differences become a cause for variations in the common potential VCOM, resulting in the generation of a flicker.

[0010] Accordingly, it is desirable to provide a data driver for a liquid-crystal display device, with a high density of current components, a decreased power consumption and satisfactory pixel flicker properties.

[0011] In embodiments of the present invention, each data-bus line is connected, by a short-circuiting switch, to one of the adjacent data-bus lines concerned with the same display colour, and the short-circuiting switches are turned on when the outputs of the voltage buffer amplifiers or locations between the voltage buffer amplifiers and the respective data-bus lines are in a high impedance state.

[0012] Data signals for adjacent pixels concerned with the same colour have opposite polarities, and it is highly probable that the absolute values thereof are nearly equal. Particularly, this probability is higher in a region of a background image. Hence, by turning on the short-circuiting switches, the potentials of the data-bus lines become nearly equal to the common potential of the opposite electrode of an LCD panel, whereby the current to be consumed in the voltage buffer amplifiers can be reduced further where short-circuiting switches are intermittently connected between adjacent data-bus lines.

[0013] Further, since the common potential is stabilized, flicker is alleviated, and thereby the image quality is better than in the case where short-circuiting switches are intermittently connected between adjacent data-bus lines.

[0014] In addition, since the number of short-circuiting switches is smaller than in the case where a short-circuiting switch is connected between each pair of data-bus lines, the circuit area of the data driver can be reduced.

[0015] In a simple type of embodiment of the present invention the short-circuiting switches can be arranged in a number of rows, in the plane of the device, equal to

the number of colours carried by the data-bus lines.

[0016] However, preferably the short-circuiting switches are connected through interconnecting lines arranged in first and second rows in a staggered configuration, with adjacent connected pairs on alternate rows.

[0017] With this data driver for a liquid-crystal display device, since the short-circuiting switches and the interconnecting lines for them are arranged so that their densities are nearly uniform, the circuit area of the data driver can be smaller, and a higher density of the data-bus lines can be realized.

[0018] Preferably, the short-circuiting switches are formed at one side of every other data-bus line. With this configuration, the above-described effect is further enhanced.

[0019] For a better understanding of the invention, embodiments of it will now be described, by way of example, with reference to the accompanying drawings in which:

Fig. 1 is a schematic circuit diagram showing a liquid-crystal display device of a first embodiment of the present invention;

FIGS. 2(A) and 2(B) are illustrations showing pixel voltage polarity distributions of odd and even frames, respectively;

Fig. 3 is a circuit diagram showing an output stage of the data driver of Fig. 1;

Fig. 4 is a circuit diagram showing an output stage of a data driver of a second embodiment of the present invention;

Fig. 5 is a circuit diagram showing part of a data driver of a third embodiment of the present invention;

Fig. 6 is a layout view of part in Fig. 5 lower than a short dashed line;

Fig. 7 is a waveform diagram showing operation of the output stage of Fig. 5;

Fig. 8 is a circuit diagram showing an output stage of a prior art data driver connected to data-bus lines of an LCD panel;

Fig. 9 is a circuit diagram showing an output stage of another prior art data driver;

Fig. 10 is an illustration of potentials of the data-bus lines D1 to D6 of Fig. 9 during a horizontal period; and

Fig. 11 is an illustration of potentials of the data-bus lines D1 to D6 after short-circuiting switches between the data-bus lines are turned on from the state of Fig. 10.

[0020] In the discussion of the drawings like reference characters designate like or corresponding parts throughout several views.

First Embodiment

[0021] **Fig. 1** schematically shows a liquid-crystal display device of a first embodiment according to the present invention. In Fig. 1, there is shown an LCD panel 11 having a pixel matrix in 4 rows and 6 columns for simplification.

[0022] In the LCD panel 11, a pair of opposed glass substrates, not shown, are disposed, and a gap therebetween is filled with a liquid crystal and sealed. Pixel electrodes are arranged in a matrix on one of the glass substrates, thin-film transistors are formed for the respective pixels, scan-bus lines (gate lines) G1 to G4 are formed for respective first to fourth rows of the thin-film transistors, and data-bus lines D1 to D6 are formed for first to sixth columns of the thin-film transistors, wherein the scan-bus lines G1 to G4 and the data-bus lines D1 to D6 cross each other with an insulating film interposed therebetween. On the other glass substrate, a transparent plane electrode in common with all of the pixels is formed and a common potential VCOM is applied thereto. For example, in regard to the liquid-crystal pixel C11 of the first row and the first column, a thin-film transistor T11 is connected between the pixel electrode and the data-bus line D1, the gate of the thin-film transistor T11 is connected to the scan-bus line G1, and the common potential VCOM is applied to the opposite electrode of the liquid-crystal pixel C11.

[0023] The data-bus lines D1 to D6 of the LCD panel 11 are connected to the outputs of the data driver 10, and the scan lines G1 to G4 of the LCD panel 11 are connected to the outputs of a scan driver 12.

[0024] A control circuit 13 receives a video signal VS, a pixel clock CLK, a horizontal sync signal HSYNC, and a vertical sync signal VSYNC, and generates timing signals to provide to the data driver 10 and the scan driver 12, and provides a video signal to the data driver 10.

[0025] The scan-bus lines G1 to G4 are sequentially activated by the scan driver 12, while signal charges for pixels on a selected row are renewed by the data driver 10. The data driver 10 simultaneously provides display data signals for a row onto the data-bus lines D1 to D6, and renews the signals each horizontal period.

[0026] The data driver 10 drives in a dot-inversion fashion. That is, the data driver 10 provides analog gradation voltages according to display data in such a way that the voltage polarities of adjacent data-bus lines are inverse or opposite to each other and the voltage polarity of each data-bus line is inverted every horizontal period. **FIGS. 2(A) and 2(B)** show the pixel voltage polarity distributions of odd and even frames, respectively.

[0027] **Fig. 3** shows the output stage of the data driver 10. The actual number of data-bus lines is, for example, 1024 x 3 = 3072, and Fig. 3 shows only data-bus lines D1 to D12 as a representative part.

[0028] The data-bus lines D1 to D12 on the LCD panel 11 are respectively connected to the outputs of voltage buffer amplifiers B1 to B12 of the data driver 10, and

each voltage buffer amplifier is constituted as a voltage follower. Each data-bus lines carries either a red (R); green (G), or blue (B) colour signal and they are arranged so that there is a signal of each colour every three lines.

[0029] Short-circuiting switches are connected between pairs of adjacent data-bus lines concerned with the same display colour. That is, the short-circuiting switch S1 is connected between adjacent R data-bus lines D1 and D4, no short-circuiting switch is connected between the next adjacent R data-bus lines D4 and D7, and a short-circuiting switch S7 is connected between the next pair of adjacent R data-bus lines D7 and D10. Likewise, a short-circuiting switch S2 is connected between adjacent G data-bus lines D2 and D5; and a short-circuiting switch S8 is connected between adjacent G data-bus lines D8 and D11. Further, a short-circuiting switch S3 is connected between adjacent B data-bus lines D3 and D6, and a short-circuiting switch S9 is connected between adjacent B data-bus lines D9 and D12.

[0030] A control circuit 13 sets the outputs of the voltage buffer amplifiers B1 to B12 into a high impedance state during each successive horizontal blanking period, and turns on all the short-circuiting switches S1 to S3 and S7 to S9.

[0031] Adjacent pixel data signals of the same colour have opposite polarities to each other, and it is highly probably that the absolute values thereof are almost the same as each other. This probability is particularly high in the region of a background image. Therefore, the potentials of the data-bus lines D1 to D12 are made almost equal to the common potential VCOM when short-circuited, and the currents consumed in the voltage buffer amplifiers B1 to B12 can be reduced to almost a half that of the case where no short-circuiting switch is connected. Further, the common potential VCOM of the opposite electrode is prevented from varying by capacitive coupling, and thereby reducing flicker compared with the case of Fig. 9. Furthermore, since the number of short-circuiting switches is half that of the case of Fig. 8, the circuit area of the data driver 10 can be reduced, enabling a higher data-bus line density to be achieved.

Second Embodiment

[0032] **Fig. 4** shows an output stage of a data driver 10A of a second embodiment of the present invention.

[0033] In this circuit, interconnecting lines L1 to L3 for connecting short-circuiting switches S1, S5 and S9 on a first row and interconnecting lines L4 to L6 for connecting short-circuiting switches S3, S7 and S11 on a second row are arranged in a staggered configuration.

[0034] In each of these first and second rows, the ends of adjacent short-circuiting switches are connected to respective adjacent data-bus lines: that is, in the first row the right-hand and left-hand ends respectively of the short-circuiting switches S1 and S5 are connected to the data-bus lines D4 and D5, and one end each of the short-circuiting switches S5 and S9 is connected to the respective data-bus lines D8 and D9, while in the second row one end each of the short-circuiting switches S3 and S7 is connected to the respective data-bus lines D6 and D7, and one end each of the short-circuiting switches S7 and S11 is connected to the respective data-bus lines D10 and D11. Thus data lines are connected two at a time to the first and second rows of switches alternately.

[0035] The short-circuiting switches S1, S3, S5, S7, S9 and S11 are controlled by the control circuit 13 in a similar manner to the above-described first embodiment.

[0036] According to the second embodiment, a similar effect to that of the first embodiment is obtained. Furthermore, since the interconnecting lines for the short-circuiting switches are arranged only in first and second rows, with a roughly uniform density of interconnecting lines, and the density of the short-circuiting switches is also roughly uniform, the area of the data driver 10A can be smaller than that of the case of Fig. 3 whilst having data-bus lines in a higher density arrangement.

Third Embodiment

[0037] **Fig. 5** shows part of a data driver 10B of a third embodiment of the present invention.

[0038] Positive-polarity voltage buffer amplifiers PB1 to PB3 are for providing higher ('H' side) voltages than the common potential VCOM (for example, 5V), while negative-polarity voltage buffer amplifiers NB1 to NB3 are for providing lower ('L' side) voltages than the common voltage VCOM. The two types of the voltage buffer amplifiers are employed, one for the 'H' side and the other for the 'L' side, to realize a narrower output amplitude so as to simplify the configuration of the device.

[0039] In order to provide the outputs of the positive-polarity voltage buffer amplifier PB1 and the negative-polarity voltage buffer amplifier NB1 to each of the output terminals T1 and T2 alternately in each successive horizontal period (1 H), transfer gates P1 and P2 are connected between the output of the positive-polarity voltage buffer amplifier PB1 and the respective output terminals T1 and T2, and transfer gates N1 and N2 are connected between the output of the negative-polarity voltage buffer amplifier NB1 and the respective output terminals T1 and T2. Transfer gates P1, P2, N1, and N2 constitute one set of changeover switches. This applies to changeover switches between other voltage buffer amplifiers and corresponding output terminals in a similar way. Between these changeover switches and the output terminals T1 to T6, the short-circuiting switches S1, S3 and S5 are connected in a similar manner to the case of Fig. 4.

[0040] **Fig. 6** shows a circuit layout of the part 20 of the circuit of Fig. 5 below the short dashed line. In Fig. 6, electrodes A to F, I to T, and U to W correspond to respective locations indicated by the same reference

characters in Fig. 5.

[0041] Each of the transfer gates of Fig. 5 has a PMOS transistor and an NMOS transistor connected in parallel to each other, and the PMOS transistors are formed in a horizontal strip-shaped region 21 and the NMOS transistors are formed in a similar, vertically adjacent region 22.

[0042] For example, the PMOS transistor of the transfer gate P1 has vertical strip-shaped source and drain electrodes A and I, and a gate drawn by a thick black line therebetween, and the PMOS transistor of the transfer gate N1 has the electrodes A and J, and a gate drawn by a thick black line therebetween. The NMOS transistors of the transfer gates P1 and N1 have portions corresponding to those electrodes, being extensions down into the NMOS transistor region 22.

[0043] The PMOS transistor of the short-circuiting switch S1 has source and drain electrodes A and U, and a gate drawn by a thick black line therebetween, the PMOS transistor of the short-circuiting switch S3 has the electrodes C and V, and a gate drawn by a thick black line therebetween, and the PMOS transistor of the short-circuiting switch S5 has the electrodes E and W, and a gate drawn by a thick black line therebetween. Likewise, the NMOS transistors of the short-circuiting switches S1, S3 and S5 have portions corresponding to those, in the NMOS transistor region 22. The electrode U is connected to the electrode D through the interconnecting line L1 on a first row, the electrode V is connected to the electrode F through an interconnecting line L4 on a second row, and the electrode W is connected to an interconnecting line L2 on the first row. In Fig. 6, these interconnecting lines L1, L4 and L2, which are in an upper wiring layer, not shown, are simply drawn.

[0044] Since the short-circuiting switches are formed at one side of every other data-bus line, and the interconnecting lines L1, L4 and L2 for connecting the short-circuiting switches are arranged only on the first and second rows between the PMOS transistor region 21 and the NMOS transistor region 22, in such a way that the density of interconnecting lines is nearly uniform, the area of the circuit 20 can be narrowed and the output terminals T1 to T6, which are considered to be part of the respective data-bus lines, can be arranged with a high density.

[0045] Referring back to Fig. 5, positive-polarity voltage selectors PS1 to PS3 are shown, each of which selects one of a range of positive-polarity gradation voltages VP31 to VP0 according to the corresponding output value of respective registers R1, R3 and R5, to apply it to the corresponding positive-polarity voltage buffer amplifier PB1 to PB3. Likewise, each of the negative-polarity voltage selectors NS1 to NS3 selects one of the negative-polarity gradation voltages VN31 to VN0 according to the corresponding output values of respective registers R2, R4 and R6 and applies it to the corresponding negative-polarity voltage buffer amplifier NB1 to NB3. A latch signal LT is provided for the clock inputs of the registers R1 to R6.

[0046] **Fig. 7** is a waveform diagram showing the operation of the output stage of Fig. 5.

[0047] The latch signal LT is a pulse issued in each cycle of 1 'H', and pixel data are latched into the registers R1 to R6 on the rise of each pulse. During each pulse period of the latch signal LT, the transfer gates P1 to P6 and N1 to N6 stay off, and a high-impedance state arises between the voltage buffer amplifiers and the output terminals. In this period, the short-circuiting switches S1, S3 and S5 are turned on, and thereby the voltages of the terminals connected by the short-circuiting switches are averaged.

[0048] The invention is not, of course, limited to the embodiments shown, and many modifications are possible. For example, the voltage buffer amplifiers may be respective source follower circuits. Further, a data driver may be formed in one piece with an LCD panel by employing thin-film transistors.

Claims

1. A data driver for a display device having an array of data-bus lines (Di), comprising voltage-buffer amplifiers (Bi) each outputting a gradation voltage, these analog gradation voltages being applied to the said data-bus lines in such a way that the voltage polarities of adjacent data-bus lines concerned with the same display colour are opposite to each other, the data driver further comprising:

   short-circuiting switches (Si) connected between pairs of data-bus lines concerned with the same display colour; and
   a control circuit (13) closing the short-circuiting switches when the outputs of the voltage-buffer amplifiers, or locations between the voltage-buffer amplifiers and the respective data-bus lines, are in a high-impedance state.

2. A data driver according to claim 1, wherein one short-circuiting switch is connected between every two adjacent same-colour data-bus lines.

3. A data driver according to claim 1 or 2, wherein the short-circuiting switches are connected through interconnecting lines (li) arranged in first and second rows, extending across the data-bus lines, in a staggered configuration.

4. A data driver according to claim 3, wherein, within each of the said first and second rows, one end of each of the said adjacent short-circuiting switches (S1, S5) is connected to a respective one of a pair (D4, D5) of adjacent data-bus lines.

5. A data driver according to claim 4, wherein the

short-circuiting switches (U-A; V-C; W-E) are formed at one side of every other data-bus line.

6. A data driver according to any of claims 3 to 5, wherein the voltage buffer amplifiers comprise positive-polarity voltage buffer amplifiers (PB_i) and negative-polarity voltage buffer amplifiers (NB_i).

7. A data driver according to claim 6, wherein each adjacent pair of voltage buffer amplifiers comprises a positive-polarity voltage buffer amplifier and a negative-polarity voltage buffer amplifier, and a set of changeover switches (P1,N1; P2,N2) is connected between the voltage buffer amplifier and its output, the switches being constituted by transfer gates each comprising a PMOS transistor and an NMOS transistor, connected to each other, an electrode (A, C, E) of the PMOS transistor of the transfer gate in the changeover switch being shared with an electrode of the PMOS transistor of the corresponding short-circuiting switch.

8. A data driver according to any preceding claim, wherein each of the said short-circuiting switches comprises an NMOS transistor and a PMOS transistor connected in parallel to the said NMOS transistor.

9. A data driver according to any of claims 6 to 8, when dependent on any of claims 3 to 5, wherein the NMOS transistors are formed in a third row and the PMOS transistors in a fourth row, and the interconnecting lines of the first and second rows are formed in a region between the said third and fourth rows.

10. A liquid-crystal display device comprising:

a data driver according to any preceding claim;
an LCD panel having a plurality of data-bus lines and a plurality of scan-bus lines;
a scan driver connected to the said plurality of scan-bus lines.

FIG.1

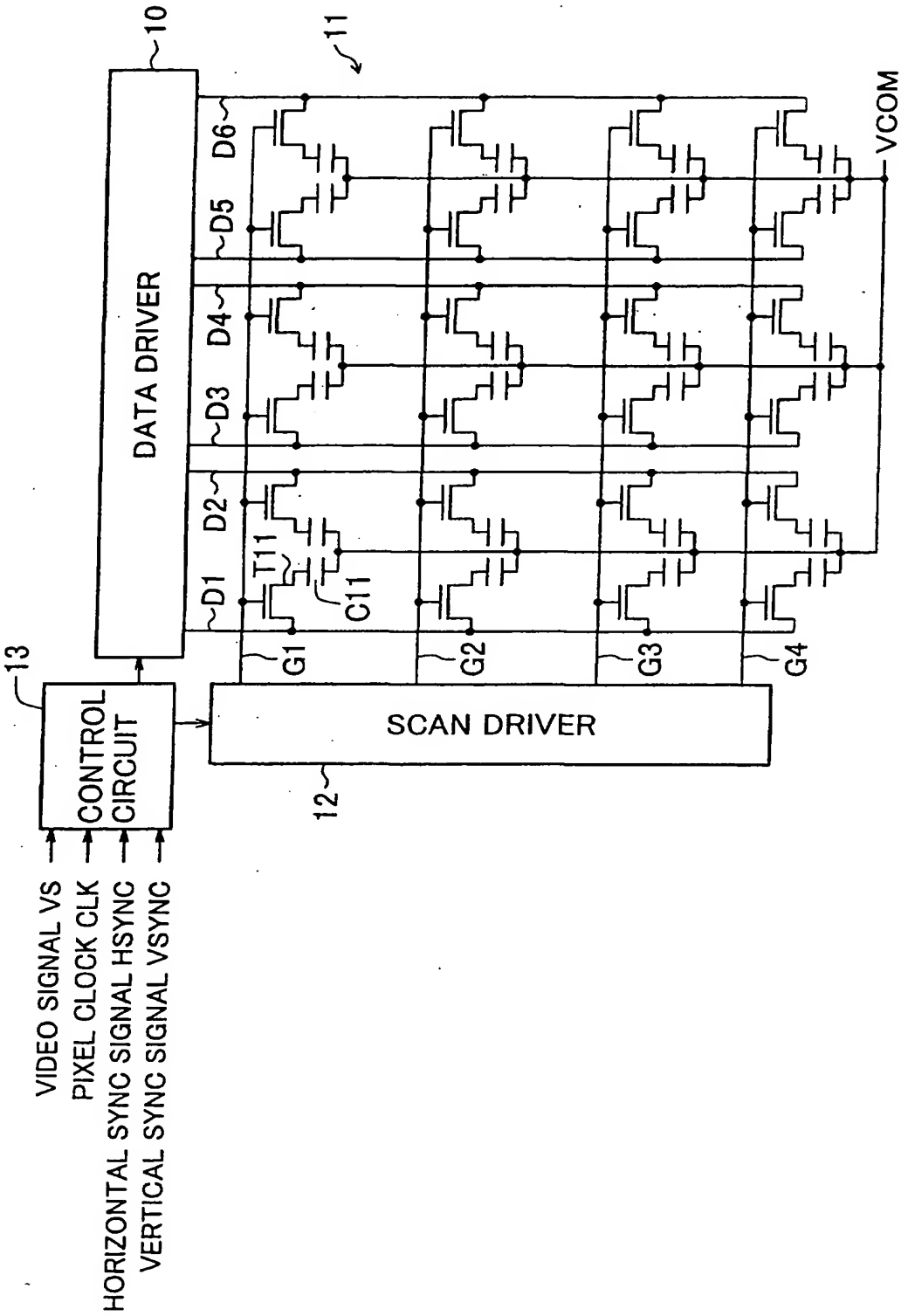


FIG.2(A)

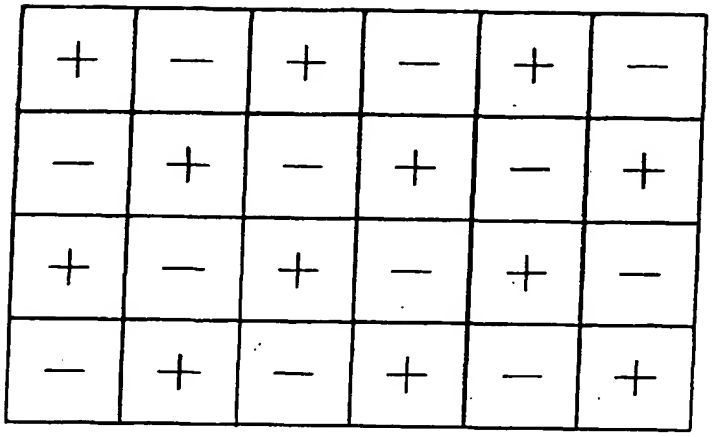


FIG.2(B)

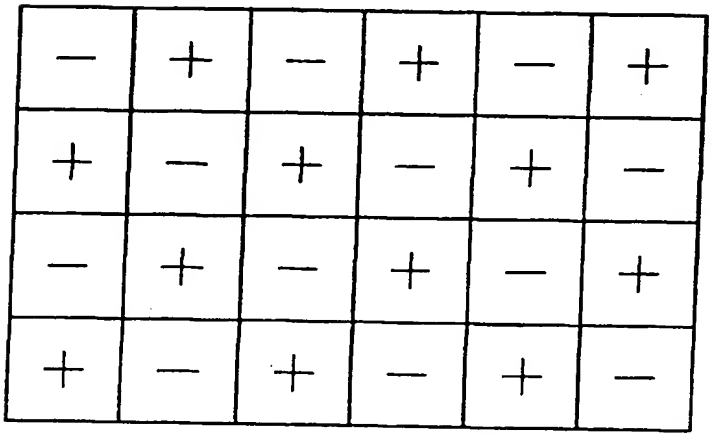
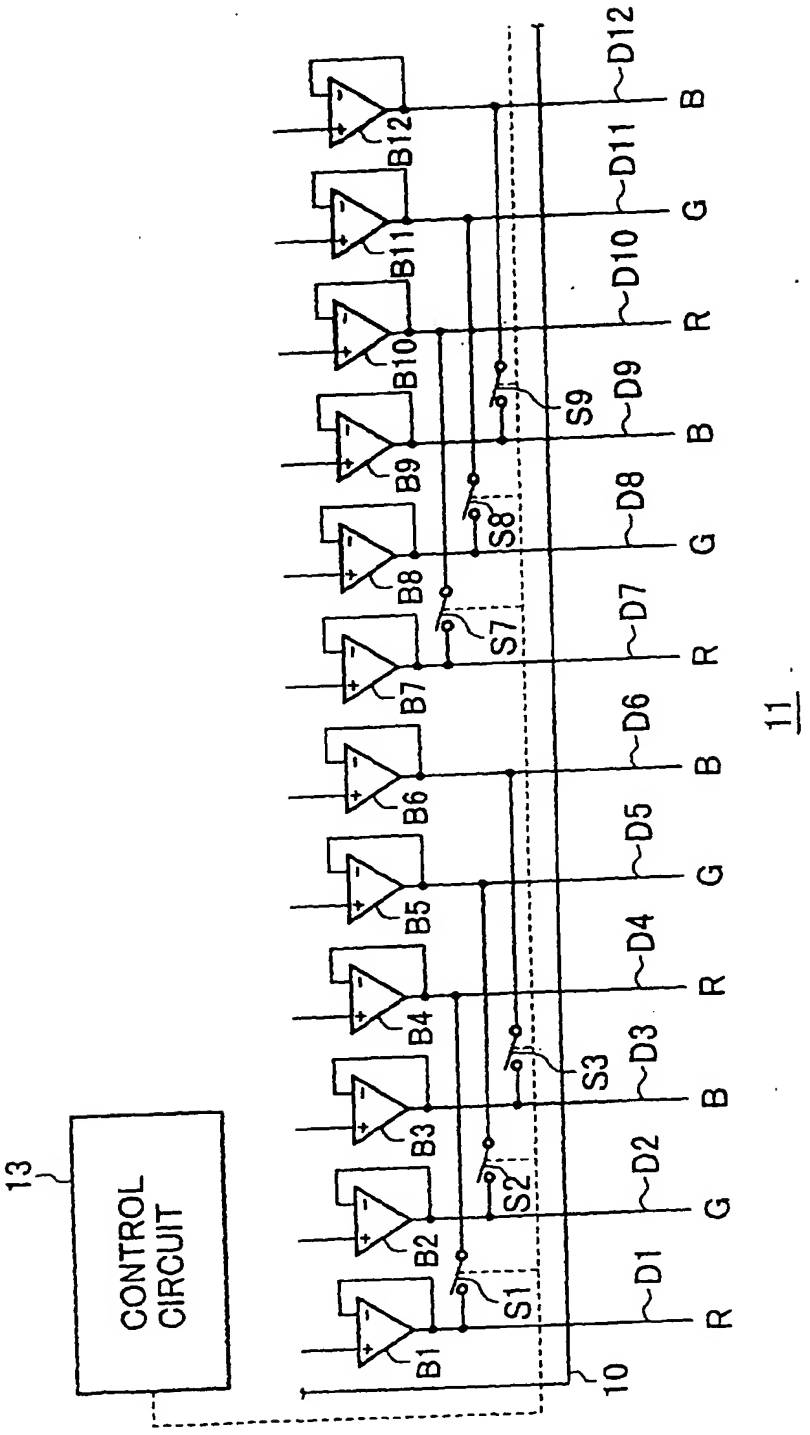


FIG.3


13
CONTROL CIRCUIT
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
S1
S2
S3
S7
S8
S9
D1
D2
D3
D4
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D6
D7
D8
D9
D10
D11
D12
R
G
B
10
11

FIG.4

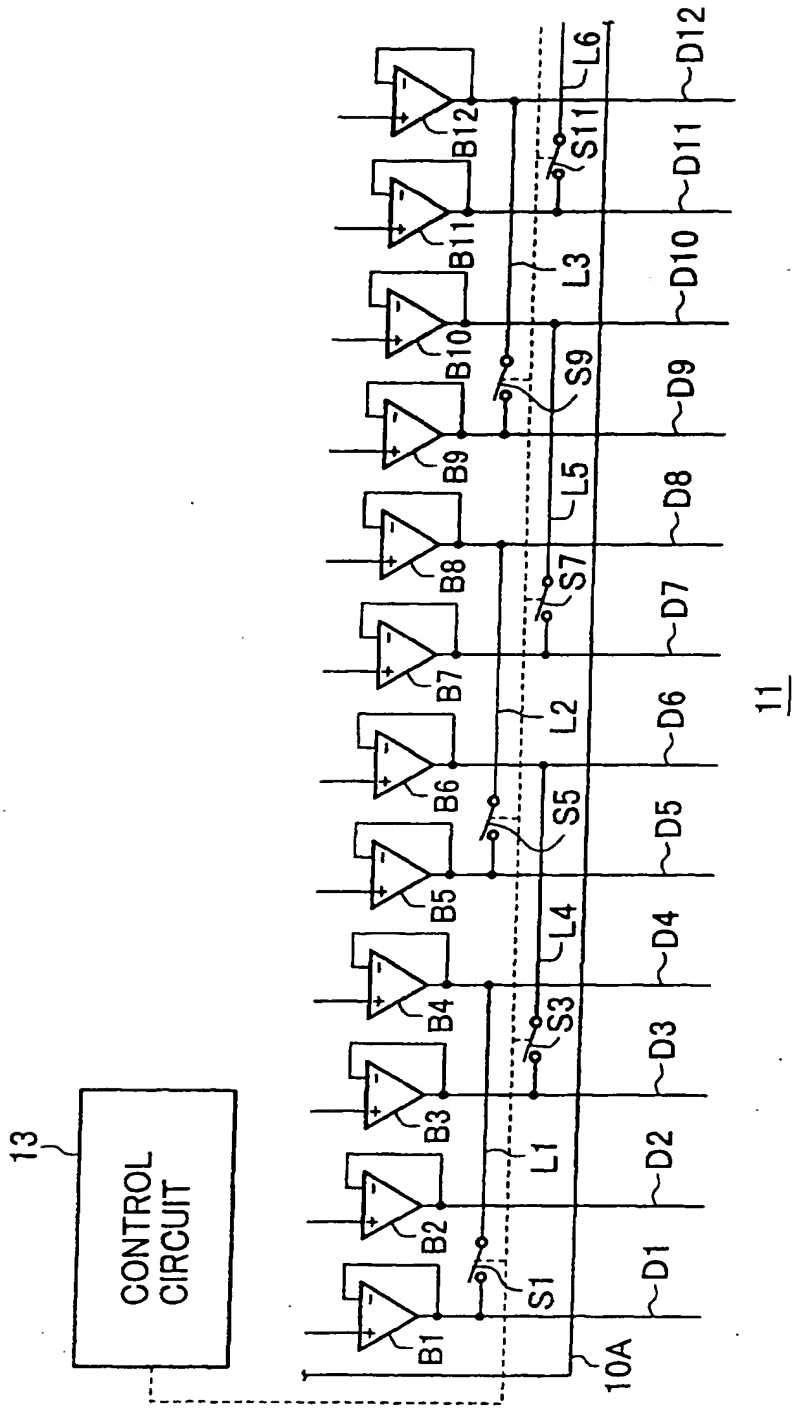


FIG.5

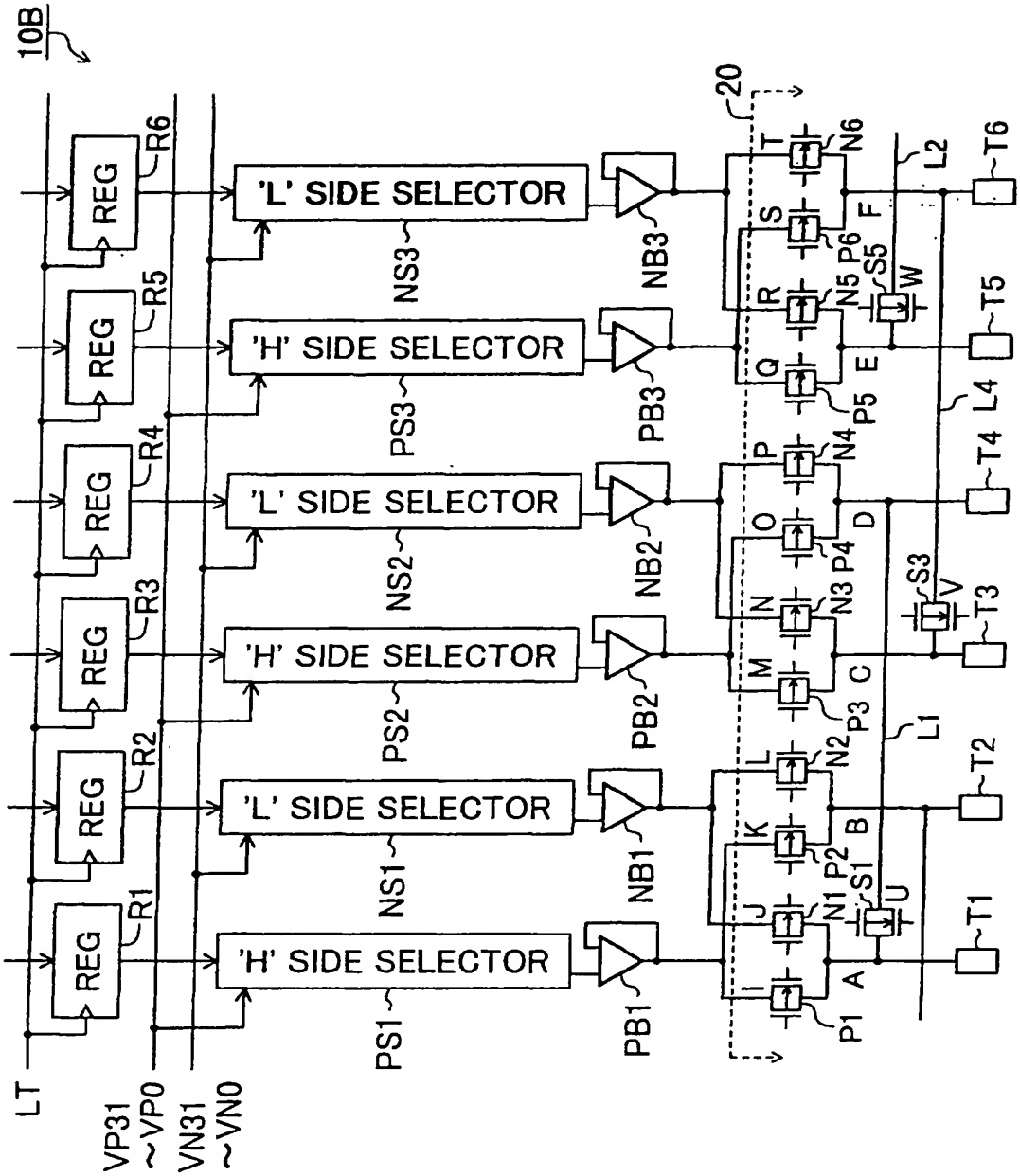

10B
20
'L' SIDE SELECTOR
'H' SIDE SELECTOR
'L' SIDE SELECTOR
'H' SIDE SELECTOR
'L' SIDE SELECTOR
'H' SIDE SELECTOR
REG
R6
R5
R4
R3
R2
R1
NS3
PS3
NS2
PS2
NS1
PS1
NB3
PB3
NB2
PB2
NB1
PB1
T
S
R
Q
P
O
N
M
L
K
J
I
N6
P6
N5
P5
N4
P4
N3
P3
N2
P2
N1
P1
S5
S3
S1
W
V
U
F
E
D
C
B
A
L2
L4
L1
T6
T5
T4
T3
T2
T1
LT
VP31
~VP0
VN31
~VN0

FIG.6

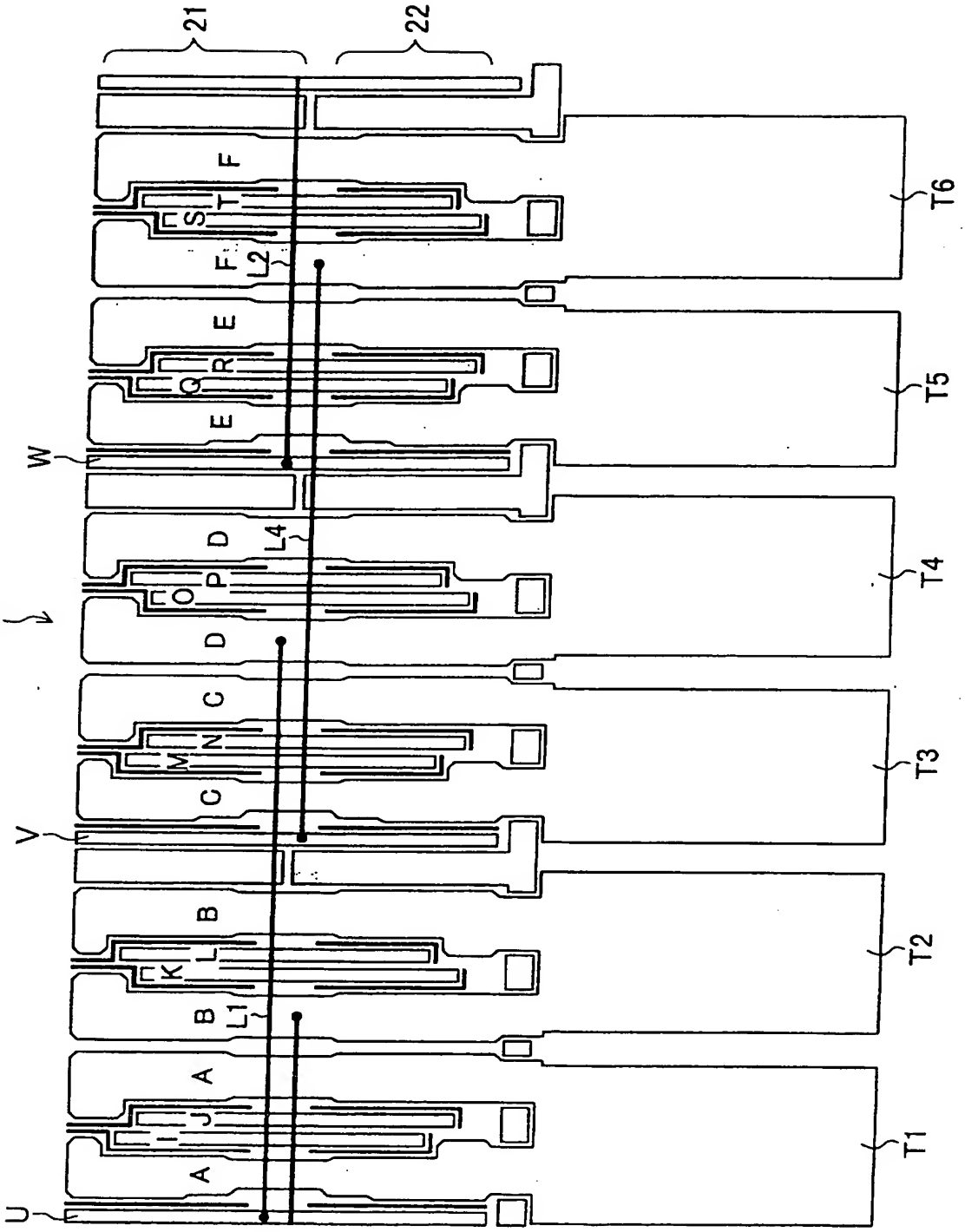


FIG.7

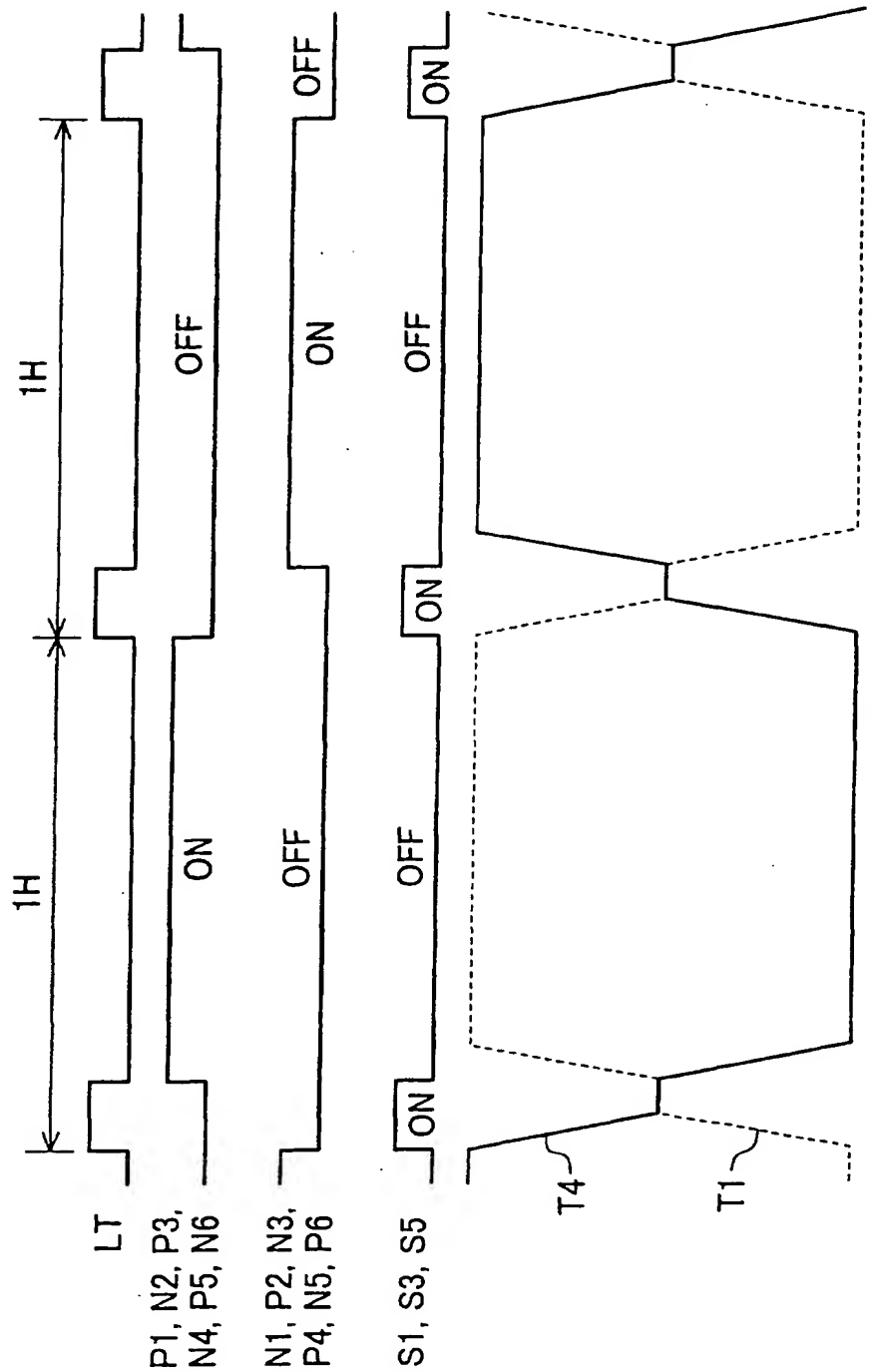


FIG.8
prior art

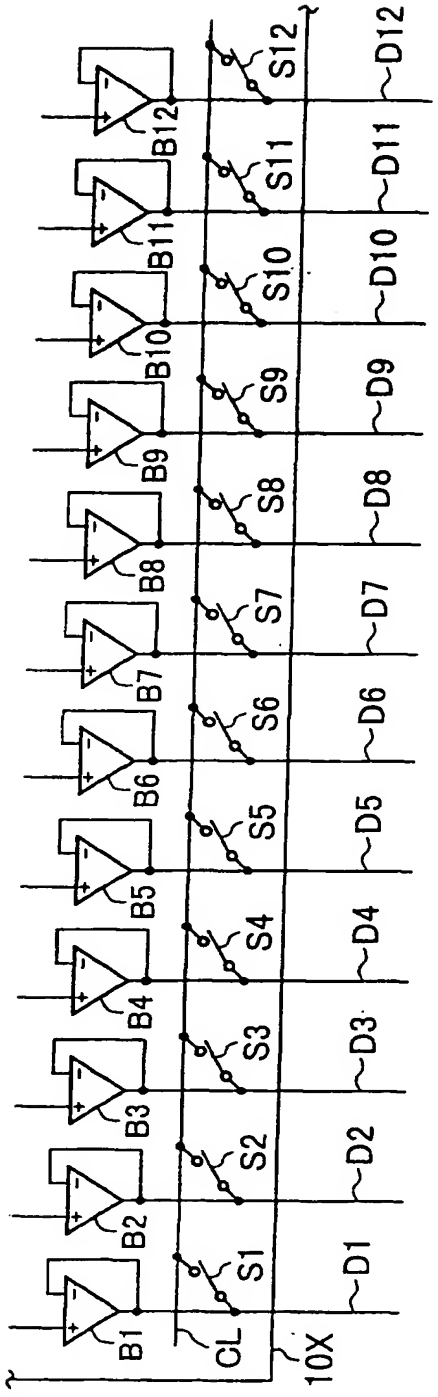


FIG.9
prior art

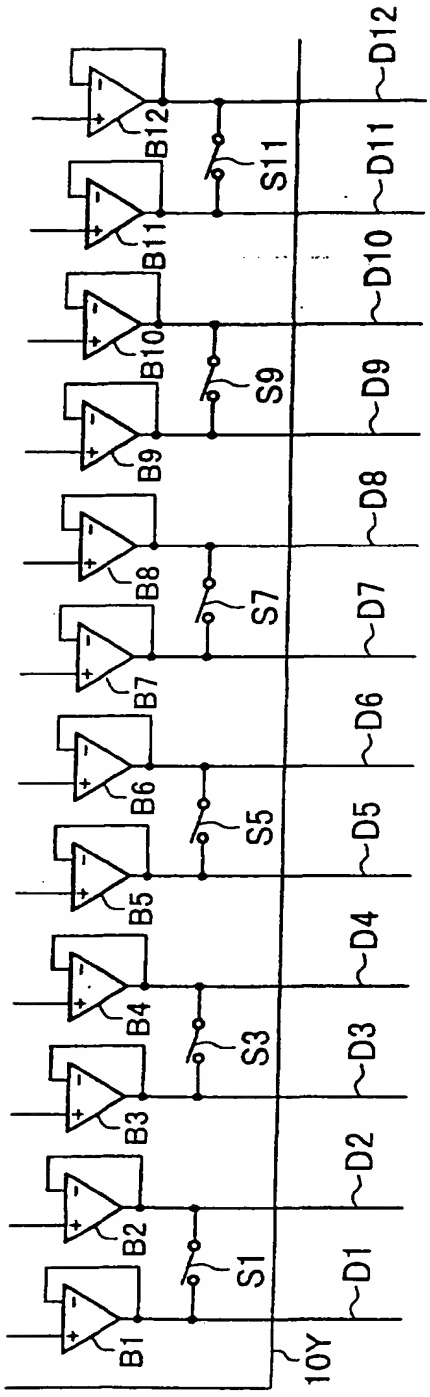


FIG.10
prior art

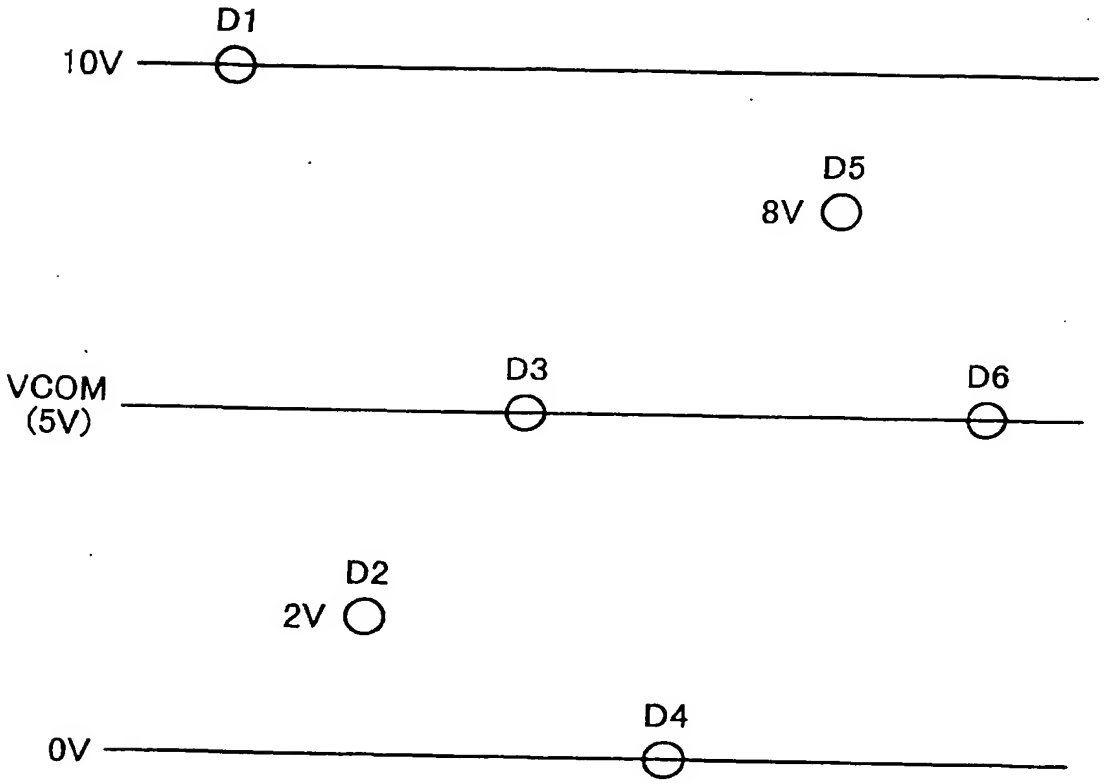
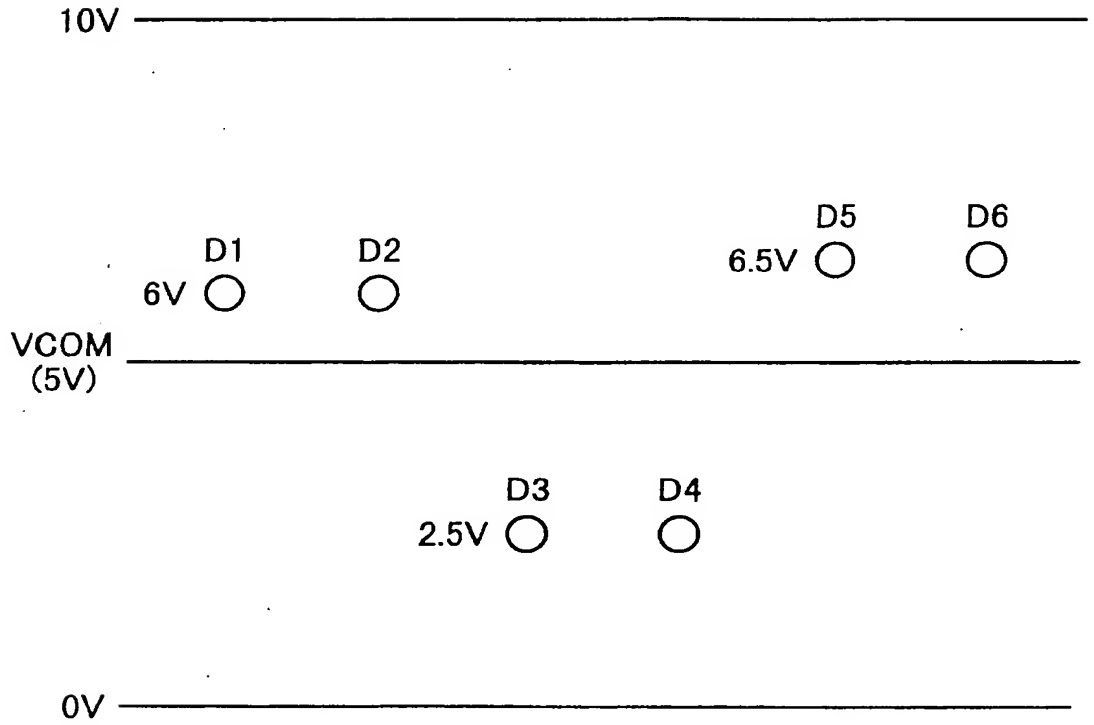


FIG.11
prior art



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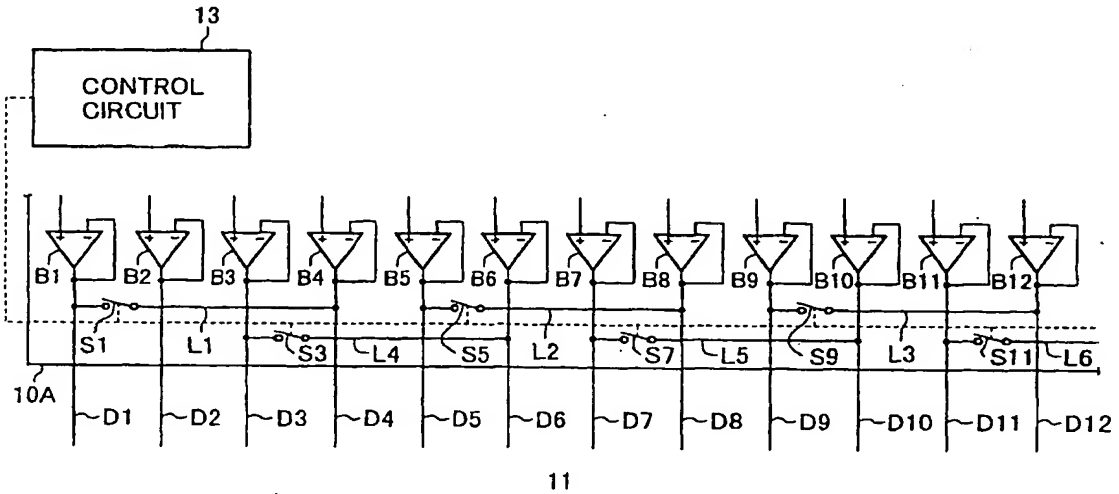
(54) Dot-inversion data driver for liquid-crystal display device

(57) In an LCD driven by a data driver 10A of a dot-inversion driving type, the outputs of voltage buffer amplifiers B1 to B12 are connected to respective data-bus lines D1 to D12 of the LC panel. The data-bus lines carry different colour signals; short-circuiting switches S1, S3, S5, S7, S9 and S11 are connected between successive pairs of data-bus lines concerned with the same display colour, and interconnecting lines L1, L2, L4 for the switches are arranged in a staggered configuration on first and second rows. These short-circuiting switches can be formed in a space-saving manner on one side of every other data-bus line, and turned on by a control circuit 13 when the outputs of the voltage buffer amplifier are in a high impedance state, i.e. in a blanking period.

FIG.4



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Application Number
EP 01 30 4785

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 November 2003	Corsi, F

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